

# SmartMX2 family

## P60C080 and P60C144

Secure high-performance contact interface smart card controller

Rev. 1 — 21 October 2010  
198210

Objective short data sheet  
PUBLIC

## 1. Introduction

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The new NXP Semiconductors SmartMX2 P60 family was created in order to cover all important market requests for state-of-the-art security chip controllers:

- Innovative and unique security measures, Common Criteria certified
- Superior transaction and personalization time
- Broadest portfolio of memory configurations with contact, dual-interface and contactless on a single platform
- Proven SmartMX reliability, interoperability and RF excellence for shortest time-to-market
- Market benchmark in view of cost-performance ratio

Further feature improvements in comparison to the existing approved SmartMX P5 family:

- Significant increases in controller and crypto performance
- Further extended CPU instructions for Java and C code
- Comprehensive hardware support for efficient and secure OS implementation
- Highest transaction and personalization speed
- Excellent power efficiency
- New-generation Fame2 crypto coprocessor for RSA/ECC
- New-generation Symmetric Block Cipher (SBC) crypto coprocessor for DES/AES
- Advanced 90 nm CMOS technology

Other important SmartMX2 P60 differentiators in the market are:

- New development tool suite, totally revised and based on an optimized close-to-product true bond-out chip emulation approach
- Broadest portfolio of certified package variations



## 2. General description

The P60C080 and P60C144 devices are members of the new SmartMX2 Family and offer with their two different EEPROM size variations a common set of functional blocks and interfaces, supporting high-performance, high-security contact applications. [Figure 1](#) shows the block diagram of the modular controller architecture consisting of the following blocks and features:

- SmartMX2 CPU with enhanced application instruction set supporting 32-/24-/16-/8-bit move, logical and arithmetic functions
- Fame2 coprocessor based on innovative power-efficient and fast architecture for optimized RSA/ECC cryptography
- SBC coprocessor interface with multiple data/key register sets now supporting both AES and Triple-DES
- ISO/IEC 7816 data transfer improved with enhanced protocol support for T=0 and T=1 protocols
- New Copy Machines supporting direct memory access (DMA) to memories and all SFRs
- Cyclic Redundancy Check (CRC) coprocessors 16-bit/32-bit
- Memory Management Unit (MMU) with 16 cache segments
- New security features especially targeting combined laser light attacks and integrity of code execution and data fetch
- Development tool suite based on approved suppliers Keil and Ashling
  - $\mu$ Vision4 user interface
  - New and high-performance emulation hardware “SmartICE series”
- High-memory SoftMasking device for code development purposes
- Common Criteria security certified high-performance crypto library supporting various algorithms
- Consequent family concept with regard to all future platforms of the P60 family

### 3. Features and benefits

#### 3.1 Product specific features

- EEPROM: choice of 80 KB or 144 KB
  - ◆ Data retention time: 25 years minimum
  - ◆ Endurance: 500000 cycles
  - ◆ Versatile EEPROM programming: 1 B to 256 B at a time
- ROM: 384 KB
- RAM: 8.125 KB (8320 B)
  - ◆ 5632 B CXRAM (including 256 B IRAM) usable for CPU
  - ◆ 2688 B FXRAM usable for Fame2 or CPU
- SmartMX2 CPU
  - ◆ orthogonal instruction set offering 32-/24-/16-/8-bit instructions optimized for secured and low power smart card applications
- Enhanced high-performance secured Public Key Infrastructure (PKI) coprocessor (RSA, ECC) Fame2
- Enhanced high-performance secured hardware support for symmetric block cipher (SBC) algorithms
  - ◆ Secured dual/triple-DES coprocessor
  - ◆ Secured AES coprocessor
  - ◆ Multiple key and data register sets supporting parallel data/key loading and calculation
- True Random Number Generator (compliant to AIS-31)
- 16-bit and 32-bit CRC coprocessor supporting fast memory verify functionality
- Memory Management Unit (MMU)
  - ◆ 16 segment cache entries and performance improvements
  - ◆ supporting integral concept for secure code fetch and execution
- Copy Machines offering data transfer between all Special Function Registers and all memory instances without CPU interaction
- Watchdog Timer supporting secure code execution
- Time Stamp Counter, Real Time Clock
- ISO/IEC 7816 contact interface (UART)
  - ◆ ISO/IEC 7816 contact interface (UART) offering hardware support for ISO/IEC 7816 T=0 and T=1 protocol stack implementation
  - ◆ Hardware support for automatic WTX generation for both ISO/IEC 7816 UART
  - ◆ continuous operation from 1.62 V up to 5.5 V supported
- -25 °C to +85 °C ambient temperature

### 3.2 Security features

- Outstanding Glue Logic chip layout approach:
  - ◆ Most efficient and proven protection against reverse engineering
  - ◆ Based on avoidance of any logical layout block recognition
- Secure Fetch (Code and Data)
- Active and dynamic shielding
- Enhanced security sensors:
  - ◆ Low and high clock frequency sensor
  - ◆ Low and high temperature sensor
  - ◆ Low and high supply voltage sensor
  - ◆ Single Fault Injection (SFI) attack detection
  - ◆ Light sensors (included integrated memory light sensor functionality)
- Electronic fuses for safeguarded mode control
- Clock input filter for protection against spikes
- Power-up and power-down reset
- Memory security (encryption and physical measures) for RAM, EEPROM and ROM
- Memory Management Unit (MMU) including memory protection:
  - ◆ Secure multi application operating systems via two different operation modes: System mode and User mode
  - ◆ OS controlled access restriction mechanism to peripherals in User mode
  - ◆ Memory mapping up to 8-MB code memory
  - ◆ Memory mapping up to 8-MB data memory
- Built-in integral concept for secure code execution covering code fetch, MMU and CPU
- Optional disabling of ROM read instructions by code executed in EEPROM
- Optional disabling of any code execution out of RAM
- Optional Unique ID for each die
- Optional programmable card disable feature
- EEPROM programming:
  - ◆ Hardware sequencer controlled
  - ◆ Enhanced error correction mechanism
- 128-B or 264-B EEPROM for customer-defined Security FabKey:
  - ◆ Featuring batch, wafer or die-individual security data
  - ◆ Encrypted diversification features available on request
- 14 B user write protected security area in EEPROM (byte access, inhibit functionality per byte)
- 32 B write once protected security area in EEPROM (bit access)
- 32 B user read only protected security area in EEPROM (byte access)
- Total useable EEPROM for customer OS (including optional FabKey areas)
  - ◆ P60C080: 81408 bytes + above 78 bytes within protected security area
  - ◆ P60C144: 146944 bytes + above 78 bytes within protected security area
- Customer specific EEPROM initialization available

## 4. Applications

- ID cards
- Health cards
- Electronic driving licences
- Contact banking
- Digital Signature
- Conditional Access (Pay TV)
- High-security access management
- Authentication
- Trusted platform modules
- Multi-application cards

## 5. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions <a href="#">[1]</a>	Min	Typ	Max	Unit
V <sub>DD</sub>	supply voltage	Class A: 5 V range	4.5	5.0	5.5	V
		Class B: 3 V range	2.7	3.0	3.3	V
		Class C: 1.8 V range	1.62	1.8	1.98	V

[1] **Remark:** continuous operation from 1.62 V up to 5.5 V supported

## 6. Ordering information

**Table 2. Feature table (EEPROM and RAM sizes without applied implementation of MIFARE Plus and/or DESFire EV1)**

Product type	EEPROM [KB]	user ROM [KB]	total RAM [KB]	CXRAM [KB]	FXRAM [KB]	Coprocessor			MMU	Copy machines	ISO/IEC 7816 IO pads	interface option
						Fame2	DES	AES				
P60C080	80	384	8.125	5.5	2.625	yes	yes	yes	yes	2	3	ISO/IEC 7816
P60C144	144	384	8.125	5.5	2.625	yes	yes	yes	yes	2	3	ISO/IEC 7816

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
P60C080PU15 P60C144PU15	FFC	12 inch wafer (sawn; 150 μm thickness; on film frame carrier; electronic fail die marking according to SECSII format)	NAU000
P60C080PHN P60C144PHN			
P60C080PX80 P60C144PX80	PCM1.1	contact chip card module (super 35 mm tape format, 8-contact, dual source)	SOT658-1
P60C080PX81 P60C144PX81			
	Pd-PCM1.1	palladium plated contact chip card module (super 35 mm tape format, 8-contact, dual source)	SOT658-1

## 7. Functional diagram

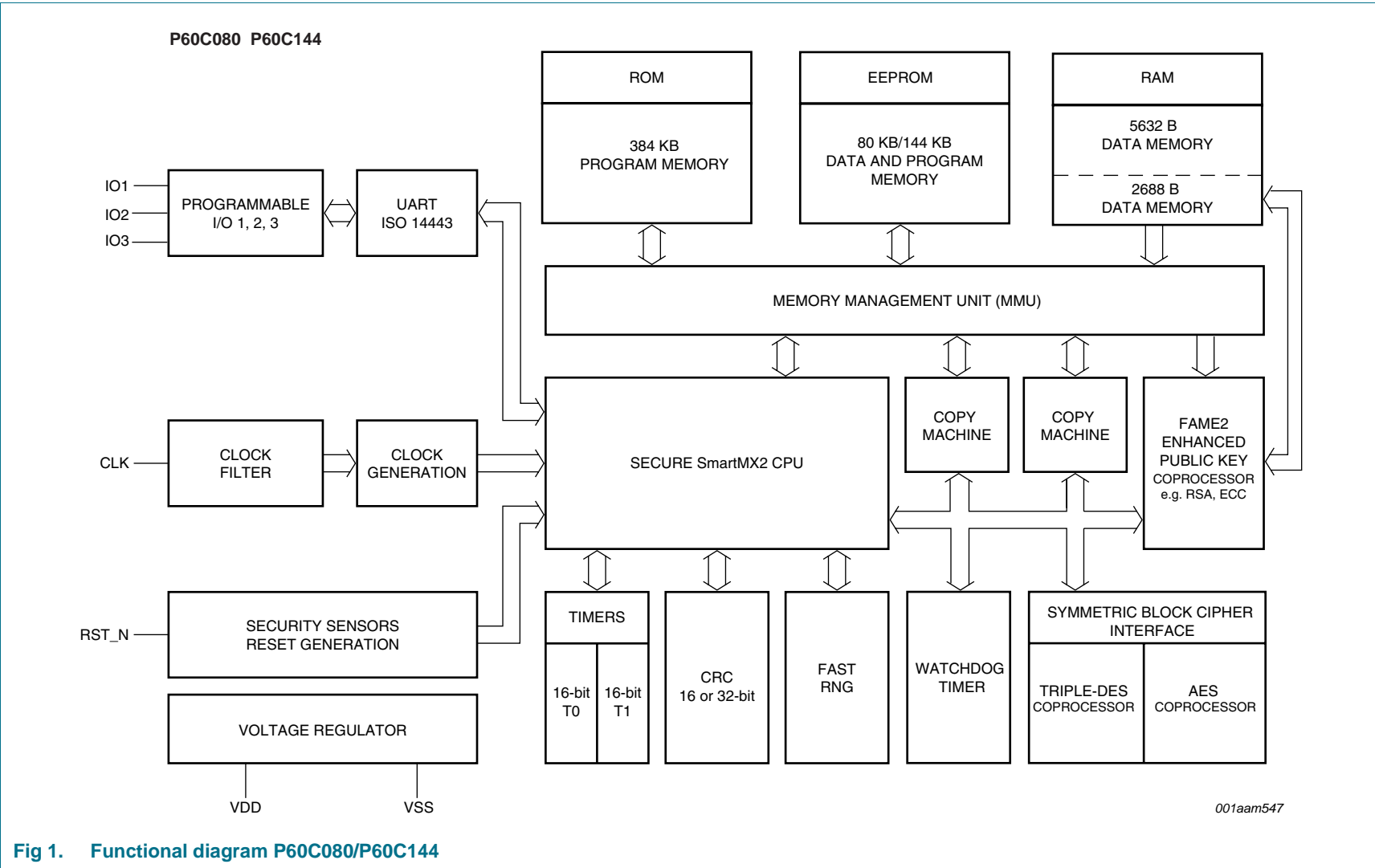


Fig 1. Functional diagram P60C080/P60C144

## 8. Abbreviations

**Table 4. Abbreviations**

<b>Acronym</b>	<b>Description</b>
AES	Advanced Encryption Standard
DES	Digital Encryption Standard
ECC	Elliptic Curve Cryptography
ICE	Integrated Circuit Emulator
RSA	Rivest, Shamir and Adleman
SECSII	Semiconductor Equipment Communications Standard 2
SFR	Special Function Register



## 9. Revision history

Table 5. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SMX2_FAM_P60C080_C144_SDS v.1	20101021	Objective short data sheet	-	-

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### 10.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 21 October 2010  
198210